REMARKS

Claims 1-9 and 11-16 are pending, with claims 1 and 11 being in independent form. Claims 1-9 and 11-16 would be canceled. Claims 17-23 would be added.

At the outset, Applicants note that new claim 17 combines the features of pending claims 1-3. Moreover, new claims 18-23 define subject matter substantially similar to that defined by pending claims 4-9, respectively. Accordingly, Applicants respectfully submit that entry of this Amendment after final would be proper, as the Amendment merely presents the rejected claims in better form for consideration on Appeal.

In the final Office Action, claims 1, 4-5, and 11-16 stand rejected for obviousness over U.S. Patent No. 5,240,867 to Suzuki et al. ("Suzuki") in view of U.S. Patent No. 5,583,367 to Blossfeld. Claims 2-3 and 6- 9 stand rejected for obviousness over Suzuki and Blossfeld in further view of U.S. Patent No. 6,063,678 to D'Anna. Applicants believe the claims, as would be amended by entry of this Amendment, are novel and inventive over the cited documents, and respectfully request reconsideration for the following reasons.

In response to Applicants' prior-raised argument that Suzuki does not disclose a ground plug and a ground connection in accordance with the claimed invention, the final Action asserts that it is understood in the art of electronics that a device operates depending only on the difference between voltages applied to the poles of the device, and that what is called ground is irrelevant for the voltage difference. While this assertion can be true for certain discrete electronic components, the statement is not true for a semiconductor device fabricated on a substrate as defined by claim 17, or as described in the cited documents. The voltage potential of the substrate in relationship to the semiconductor device must always be considered in such applications, as the substrate bias (often referred to as the back-bias) can produce effects (e.g., the body effect in MOS devices and bias and leakage effects in bipolar devices) that affect the electronic characteristics of the semiconductor devices.

For example, at col. 7, ll. 14-24, Suzuki describes an arrangement in conjunction with FIG. 5 in which a p^+ isolation region 65:

> is supplied with the most negative voltage V_{EE} used in the device. As a result, the p-n junction formed between the region 65 and the n^--type layer 64 surrounding the region 65, and the p-n junction formed between the p^--type layer 63 to which the region 65 is connected and the n^+-type substrate 61, are always biased reversely and prohibits the current supplied to the metallized layer 62 from the external voltage source from entering into the region of layer 64 above the p^--type layer 63.

Applicants' invention, as defined by claim 17, is not so limited. Moreover, Applicants respectfully assert that it would not be obvious to one of ordinary skill in the art to modify the isolation arrangement described by Suzuki to provide a ground connection on top of at least one layer on one side of the semiconductor substrate, as claim 17 requires.

D'Anna does not cure the deficiencies pointed out above with respect to Suzuki. The arrangement described by D'Anna requires that the source contact 26 of the MOS transistor always be connected to the substrate 12 via the conductive plug region 38. Applicants' invention, as defined by claim 17, is not so limited. Moreover, one skilled in the art would not be motivated to combine the teachings of Suzuki and D'Anna, as Suzuki's isolation arrangement discussed above would teach away from directly physically connecting the device terminal(s) and the substrate.

Likewise, Blossfeld does not cure the deficiencies of Suzuki and D'Anna. Blossfeld teaches an arrangement in which a semiconductor chip is connected to a ground connection via the substrate of the semiconductor chip, and in which the input signals pd1 and pd2 are not referred to the ground connection. Accordingly, Blossfeld would teach away from an arrangement in which a ground connection is provided on top of at least one layer on one side of the semiconductor substrate, and in which an electrically conductive connector interconnects the ground connection and the device via a metal plug, as claim 17 requires.

For the foregoing reasons, Applicants believe entry of this Amendment would put the application in condition for allowance. Thus, it is respectfully requested that this Amendment be entered, and a Notice to this effect be provided. If any questions remain, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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Date: February 24, 2003

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